K16U 0167

Reg. No. : .....

Name : .....

VI Semester B.Sc. Degree (CCSS – Reg./Supple./Improv.) Examination, May 2016

Core Course in Computer Science

6B15 CSC : COMPUTER ORGANIZATION

Time : 3 Hours Max. Weightage : 21

SECTION – A

Answer **all** questions. Weightage for a Bunch of **4** questions is **1**.

1. _____ contains the memory address of the next instruction to be executed.

   a) PC b) IR c) MAR d) MDR

2. The two phases of executing an instruction are

   a) Instruction decoding and storage

   b) Instruction fetch and instruction execution

   c) Instruction execution and storage

   d) Instruction fetch and instruction processing

3. In reverse polish notation, expression A*B + C*D is written as

   a) AB*CD*+ b) A*BCD*+

   c) AB*CD+* d) A*B*CD+

4. The communication between the components in a microcomputer takes place via the address and

   a) I/O bus b) Data bus

   c) Address bus d) Control lines

P.T.O.

5. An interface that provides I/O transfer of data directly to and form the memory unit and peripheral is termed as

a) DDA
b) Serial interface
c) BR
d) DMA

6. A Stack-organized Computer uses instruction of

a) Indirect addressing
b) Two-addressing
c) Zero addressing
d) Index addressing

7. Cache memory acts between

a) CPU and RAM
b) CPU and Hard Disk
c) ROM and RAM
d) None of these

8. What characteristics of RAM memory makes it not suitable for permanent storage ?

a) Too slow
b) Unreliable
c) It is volatile
d) Too bulky

(2×1=2)

SECTION – B

Answer **any five** questions. Weightage **1** for **each**.

9. What is Computer Organization ?

10. What you mean by gray code ?

11. Define a bus.

12. What is asynchronous transmission ?

13. Differentiate among direct mapping and associate mapping.

14. What is meant by Input-output processor ?

15. Briefly explain bit-Oriented Protocol.

16. Give a brief note on Address space and Memory space.

(5×1=5)

SECTION – C

Answer **any five** questions. Weightage **2** for **each**.

17. What are functional units ? Discuss the basic functional units of a computer.

18. Explain about floating point representation.

19. Define interrupt. Why priority of interrupt is required ? How it is restored ?

20. List the differences between a subroutine call and an interrupt.

21. Define hit ratio and explain its significance.

22. Differentiate between virtual memory and cache memory.

23. What are the major characteristics of a RISC processor ?

24. Explain how DMA controller communicates and transfers data between the peripheral devices and RAM. **(5×2=10)**

SECTION – D

Answer **any one** question. Weightage **4** for **each**.

25. List different addressing modes. Explain in detail.

26. Discuss the different mapping techniques used for cache memory. What is the need of mapping techniques ? **(1×4=4)**
