K20U 1273

Reg. No. : .....

Name : .....

III Semester B.Sc. Degree (CBCSS – Sup./Imp.) Examination, November 2020
(2014 – '18 Admns)
GENERAL COURSE IN COMPUTER SCIENCE
3A12CSC – Digital Electronics

Time : 3 Hours Max. Marks : 40

SECTION – A

1. One word answer. **(8×0.5=4)**
   a) 1101_2 = ———$_{10}$.
   b) The output of an OR gate with three inputs, A, B and C is LOW when _____
   c) If A and B are inputs to a half adder then its sum output is _____
   d) 57_{16} = _____ $_2$.
   e) A digital multiplexer is a combinational circuit that selects _____
   f) S-R type flip-flop can be converted into D type flip-flop if S is connected to R through _____
   g) Storage capacity of a register is _____
   h) Number of flip flops required to implement a modulo-6 Johnson's counter is _____

SECTION – B

Write short notes on **any seven** of the following questions. **(7×2=14)**

2. Generate the binary sequence for the decimal numbers 64 through 75.
3. What is overflow condition in signed arithmetic ?
4. Illustrate how AND-OR logic can be used for implementing SOP expressions.
5. Use NAND gates to implement the expression X = A′ + B.

P.T.O.

6. Design a 1×4 DEMUX.

7. Differentiate half adder from a full adder.

8. Compare Latches and Flip Flops.

9. Draw the logic circuit for a master slave J-K flip flop.

10. How a shift register counter differs from a basic shift register ?

11. Compare a ring counter from a Johnsons counter.

SECTION – C

Answer **any four** of the following questions : **(4×3=12)**

12. Find the hexadecimal equivalent of the following binary numbers.
    a) 1101110011.011_2 b) 101101110101.00110100_2

13. Perform subtraction using 2's complement method.
    a) $110110_2 - 100101_2$ b) $100100_2 - 111000_2$

14. With suitable waveform, truth table and logic symbols, explain basic gates.

15. Design an 8×1 MUX.

16. Give any four comparisons between synchronous and asynchronous counters.

17. With neat diagram explain the working of a parallel in serial out shift register.

SECTION – D

Write an essay on **any two** of the following questions : **(2×5=10)**

18. Establish NOR and NAND gates as Universal logic element.

19. Design an even parity generator/checker for the data 10100.

20. With the help of neat diagram and waveform, explain a synchronous decade counter.

21. Explain the working of a universal shift register with relevant diagram.