



Reg. No. :

Name :

II Semester B.Sc. Degree (CBCSS – Supplementary/Improvement)
Examination, April 2020
CORE COURSE IN PHYSICS
2B02 PHY : Electronics – I
(2014-2018 Admissions)

Max. Marks : 40

Time : 3 Hours

SECTION – A

All questions are to be answered – Very short answer type – **Each** question carries 1 mark.

1. The base of a transistor is doped.
2. A JFET is a driven device.
3. Convert 4265_8 into binary.
4. With a NAND latch a low R and a low S produce a condition.

SECTION – B

7 questions are to be answered. Short answer questions – **Each** question carries 2 marks.

5. What is faithful amplification ? What are the basic conditions in order to obtain the same ?
6. State De Morgan's theorem.
7. What do you mean by overflow and underflow ?
8. What is the need of biasing a transistor ?
9. What is the difference between JFET and bipolar transistor ?
10. Why NAND gate is called a universal gate ?



11. What is pinch off voltage in JFET ?
12. Explain AND gate with 2 input terminals.
13. What is the decimal number for 1111.01 ?
14. What do you mean by operating point ?

SECTION – C

Four questions are to be answered – Short essay/problem type – **Each** question carries **3** marks.

15. What is meant by dc load line of a transistor circuit ? Explain saturation region, cutoff region and active region of a transistor characteristics.
16. Explain the function of XOR gate with the help of a diagram. Draw the truth table for a 3-input XOR gate.
17. What is meant by odd parity and even parity ?
18. The device parameters for n-channel JFET are :
Maximum current $I_{DSS} = 10 \text{ mA}$, pinch off voltage $V_p = -4 \text{ V}$. Calculate the drain current for $V_{GS} = 0, -10 \text{ V}, -4 \text{ V}$.
19. In a transistor circuit, collector load is $4 \text{ k}\Omega$ where as the zero signal collector current is 1 mA . Calculate (a) the operating point if $V_{CC} = 10 \text{ V}$ (b) What will be the operating point if $R_{CC} = 5 \text{ k}\Omega$.
20. The collector leakage current in a transistor is $250 \mu\text{A}$ in CE arrangement. If the transistor is connected in CB arrangement, what will be the leakage current ?
Given $\beta = 100$.

SECTION – D

Two questions are to be answered – Long essay type – **Each** question carries **5** marks.

21. Explain the working and characteristics of CE amplifier.
22. Explain construction and working of a JFET.
23. Describe positional number system. What is the general form of a positional number system ? Explain binary, decimal and hexadecimal number system.
24. Explain the working of half adder and full adder using logic gates.