K20U 0100

Reg. No. : .....

Name : .....

VI Semester B.Sc. Degree (CBCSS-Reg./Supple./Improv.)
Examination, April 2020
(2014 Admission Onwards)
CORE COURSE IN COMPUTER SCIENCE
6B15CSC : Computer Organization

Time : 3 Hours

Max. Marks : 40

SECTION – A

(8×0.5=4)

One word answer.

1. a) An interrupt is a request from an I/O device for service by memory (TRUE/FALSE)

   b) Information transfer from one register to another is designated in symbolic form by means of _____ operator.

   c) The register where the serial information from the printer is stored in

   d) Which holds the present micro-instruction while the next address is computed and read from memory ?

   e) The hardware components used between the CPU and peripherals to supervise and synchronize all input and output transfers is

   f) _____ command is used to test various status conditions in the interface and the peripheral.

   g) The number of bits in the _____ field is equal to the number of address bits required to access the cache memory.

   h) CAM stands for

SECTION – B

(7×2=14)

Write short notes on **any seven** of the following questions.

2. What are registers ?
3. What is the need of Program Counter ?

P.T.O.

4. What is interrupt cycle ?
5. What is micro instruction ?
6. What are three address instruction ?
7. Mention any two characteristics of CISC.
8. Which are the ways that computer buses can be used to communicate with memory and I/O ?
9. What is data transparency ?
10. Differentiate synchronous and asynchronous bus.
11. What is strobe control ?

SECTION – C

Write short notes on **any four** of the following questions. **(4×3=12)**

12. How floating point numbers are represented ?
13. What are the phases in instruction cycle ?
14. Discuss indirect address mode.
15. Compare isolated and memory mapped I/O.
16. Discuss memory connection to CPU.
17. Explain loosely coupled system.

SECTION – D

Write short notes on **any two** of the following questions. **(2×5=10)**

18. Explain the working of any five memory reference instructions.
19. Discuss general register organization of CPU.
20. Discuss a typical asynchronous communication interface.
21. Discuss multistage switching network.
